Ultra-Low Power Chip-to-Chip Communications

Design Review 2

ECE6332

Fall, 2013

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# Introduction

Since the project proposal was submitted a great deal of progress has been made in physical layer (buffer and driver) design and chip-to-chip channel model. In addition power reduction techniques have been successfully applied to much of this design, providing as much as 6 order of magnitude improvement in leakage power during inactive periods.

Unfortunately, the portion of the project suggested in design stages 3 and 4 (bus arbitration and system integration) has been abandoned due to a lack of knowledge of synthesis tools and the availability of common hardened SPI-core RTL. For the remainder of the project we will focus on optimizing our buffer and driver designs for the channel they are to be implemented around and measuring the ability of the circuit to both reject noise at its input and drive sufficiently strong values onto the bus at its output.

The ultra-low power contribution of this work will be contained primarily in the physical network layer, and will be justified primarily using the improvements in buffer/drive power relative to the SPI core both in active and sleep modes.

# Paper Summaries

### Low power Schmitt Trigger

Al-Sarawi, S.F., "Low power Schmitt trigger circuit," *Electronics Letters* , vol.38, no.18, pp.1009,1010, 29 Aug 2002

This paper describes the basic design of a Schmitt Trigger and the addition of an NMOS/PMOS or both, into the pull up/down networks, respectively, for the purpose of reducing circuit power. These triggers have a lower frequency operation, but this is an acceptable tradeoff for the power reduction.

Three designs are shown in the paper describing how the amount of hysteresis can be selected by adding or removing specific transistors. This paper helped us to understand that we want to use a Schmitt Trigger in our input buffer design as well as how to customize the circuit to suit our particular needs.

Adding this type of circuit is important to our design because it filters unwanted noise from the outside of the chip before it enters the logic and registers, which increases the overall robustness of the circuit.

### CMOS Schmitt Trigger

*CMOS Schmitt Trigger—A Uniquely Versatile Design Component*. N.p.: Fairchild Semiconductor, June 1975. PDF. http://www.fairchildsemi.com/an/AN/AN-140.pdf

This paper describes a more advanced Schmitt Trigger design that became similar to our final design. The paper shows it operating at widely varying voltages, which we found to be a very important attribute.

This paper’s design used coupled inverters at the output of the Schmitt Trigger. In the case of the paper, it further filters unwanted transitions from the transmission line, increasing the robustness of the circuit. We chose against this, as it would reduce performance, and still does not level convert the voltage to a lower voltage to be used for the logic inside the chip.

# Design Progress Update

In this section we summarize progress on the design and update the remaining tasks and goals affiliated with the project accordingly.

## Chip-to-Chip Channel Modeling

As a part of design review 1 the following chip-to-chip channel model was proposed:

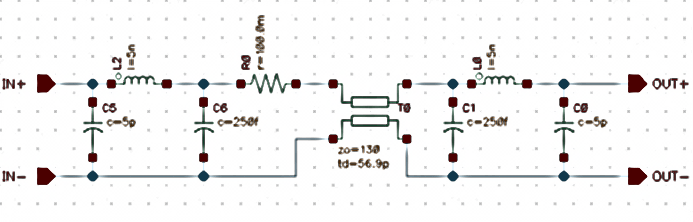


Figure 1: Chip-to-Chip Channel Model

### Model Explanation

In the circuit above, C5 and C0 represent pad capacitance, L2 and L0 bond wire inductance, and C6 and C1 pin capacitance. Resistor R0 and the transmission line represent a trace model. R0 and Z0 of the transmission line are approximated based on a worst-case physical trace length of 10cm and typical width of 10 mils (0.001in). It is important to consider the effect of the transmission line in this circuit, but also important to realize why large lumped elements are also present.

### Effects of the Transmission Line

The transmission line is a simplified model of large cascaded LC networks in which it is advantageous to calculate capacitance and inductance per unit length as opposed to considering these values as lumped elements. This is primarily relevant in short wavelength (high frequency) circuits where differentials are formed across unit elements of the line. The characteristic impedance (Z0) represents the ratio of unit inductance to capacitance in the element and along with the physical length completely characterizes the element.

It is important to recognize that Z0 is not an ohmic resistance, and in fact R0 represents this DC resistance of this line (less than 1Ω). Instead the impedance of the line is a useful consideration only when the line is of a length comparable to the wavelength of the signal being propagated. Here the elements in the cascaded LC networks are exposed to more significant differentials across them. For practical purposes we will say that we are to consider this phenomenon when:

In addition we know:

Thus, regardless of our characteristic impedance, for a physical length of 10cm we expect to not need to consider the effects of the transmission line element on our circuit until f ≥ 136.8MHz. From this we can approximate the order of magnitude of the minimum average active power (α=0.5, VDD=0.5V) of the circuit for frequency regions where we would need to consider the transmission line’s effect significantly:

We will consider this out of the range of acceptable power consumption for the low-power applications this work considers, where system consumption is less than 3 orders of magnitude smaller than this figure [1] [6]. For this reason the larger lumped elements, representing pad, bond-wire, and pin parasitics, are included for their effects on lower-frequency operation.

### Design Considerations

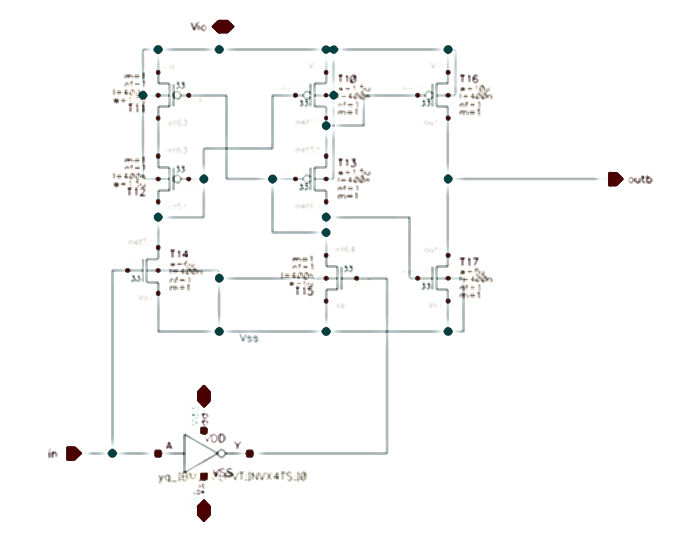
The important consideration to take away from this consideration is that when sizing the driver we should aim for the minimum size to achieve a critical propagation time for a high-to-low/low-to-high transition. This is an alternate route to the typical HF driver design technique of matching the driver output impedance to the transmission line’s characteristic impedance. Based on preliminary calculations this may results in as much as a 50% reduction in output buffer size for low-frequency applications in 130Ω FR-4 mediums.

## Level Converter Design

### Design Decisions in the Level Converter

The level converter that we designed began as a simple cross coupled PMOS level converter with an inverter between the NMOS transistors in the pull down network. We had decided earlier that we wanted a design that would be compliant if possible. This required us to find a design that would allow conversion from 500mV to 3.3V in a single stage, as extra stages will increase both active power and leakage, which go against our design goals.

We later added two PMOS transistors into the pull up network that act similarly to diodes in this circuit, allowing for a wider voltage change within this circuit. We used high voltage transistors for the actual level converter, while using the logic voltage on the inverter between the NMOS transistors. The output of the cross coupled PMOS transistors were then connected to separated PMOS and NMOS transistors, acting like an inverter, but with separate inputs, as this allows both of them to turn fully on and off.

  
Figure : Level Converter Design

### Operation of the Level Converter

The level converter operates by turning on one of the NMOS while simultaneously turning off the other NMOS. The NMOS that has been turned on pulls the gate of the opposite PMOS down, turning it on and pulling its drain high, causing a feedback loop, as the left and right side of the circuit are logically inverted.

The two transistors connected to the output then either pull up or pull down the output, depending on the input. The output will be inverted from the input in this circuit’s case, as we chose to design the output driver separate from this circuit, and the output buffer has an inverting design.

## Output Driver Design

A number of intermediate conclusions, which occurred both during the design space exploration and power reduction stages, revealed the possibility for significant driver leakage reduction across a wide range of operating voltages. The idea of implementing a low-speed communications in HVT devices for low leakage during inactivity, and correspondingly slow speed during operation was already being considered at the time of the project proposal, but was further extended in this work.

In addition, the implementation of a flexible wide-range level converter for use in the input buffer was leveraged in producing a flexible output-drive topology with low-voltage shutdown (tri-state) capabilities. This design was implemented and simulated in IBM130 technology using a mix of LVT standard cells operating in the near-threshold region and 3.3V HVT devices operating from super to deep-sub threshold at the output.

### Simple Output Buffer Design

A simplistic output buffer capable of operating at output voltage (VIO) of 0.5-3.3V was designed and simulated in IBM 130nm technology.

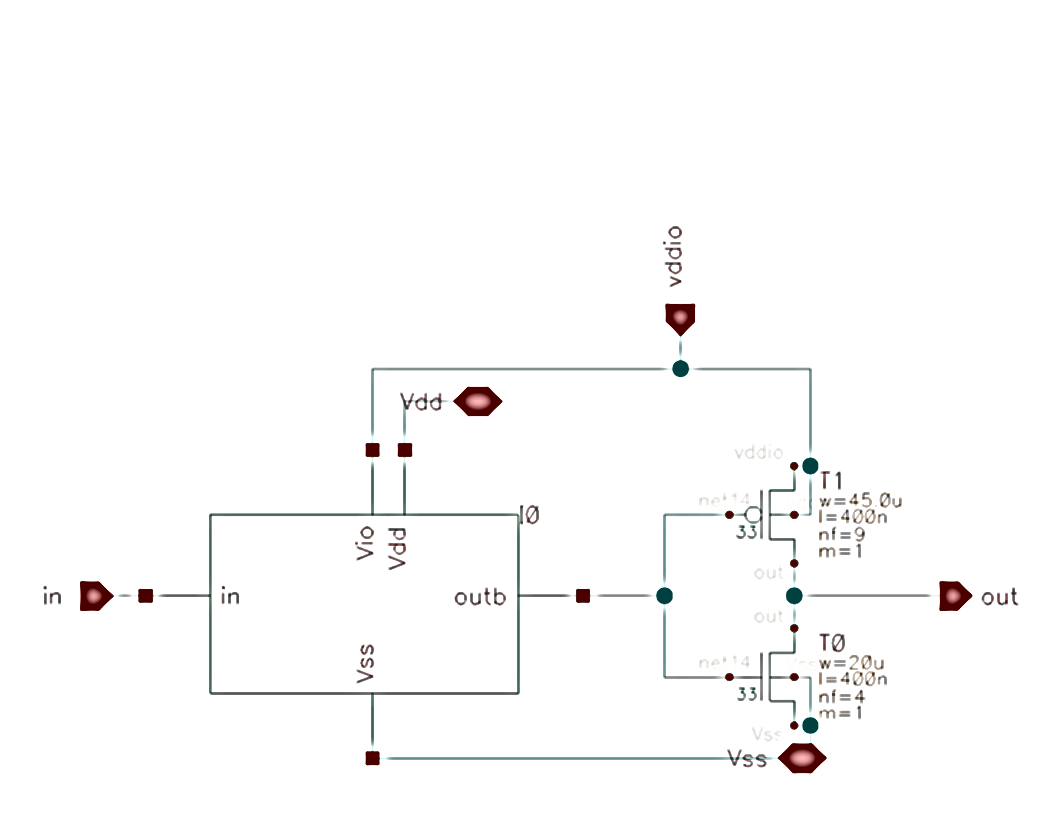


Figure 3: Simple Flexible Output Buffer Design

In this design the level converter’s inverted output is passed to the output driver (inverter) composed of devices T0 and T1. The output sizes have been determined such that the output is HF matched at 130Ω. Note that the output is always driven, and thus either T0 or T1 is always leaking. When the output voltage is low (~500mV) these 3.3V transistors are in deep sub-threshold operation and leak relatively little. Nonetheless, this leakage is avoidable and in circuits such as this, which often experience incredibly sparse usage, preferable for maximizing overall system power.

### Final Buffer Design

In response to this need for low-power shutdown and the targeted design space of low-throughput operation in ultra-low power regimes we sought to improve the active and leakage currents of this circuit by way of the addition of control logic for output shutdown and short-circuit time minimization.

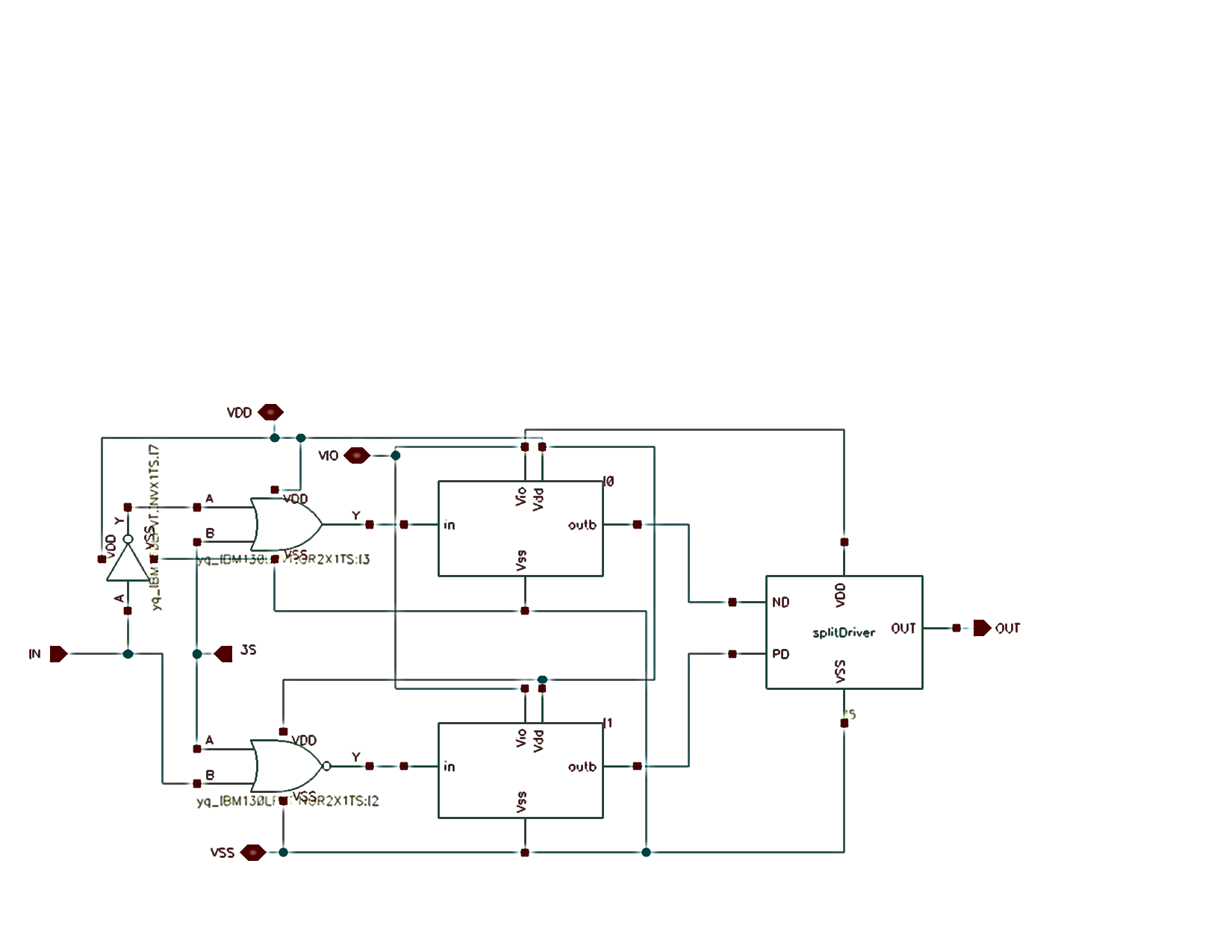


Figure 4: Top-Level Output Driver Schematic

In Figure 4 the addition of standard cell logic and a split P-drive, N-drive buffer allows for tri-state control of the output pin. When the tri-state input is high the N-drive input to the split driver circuit is driven low and the P-drive input is driven high, regardless of the state of the in pin. This circuit does require twice the level-converter logic, but the leakage of this circuit is relatively small compared to that of the final output driver stage if mismanaged. The design for the split P/N driver is included below.

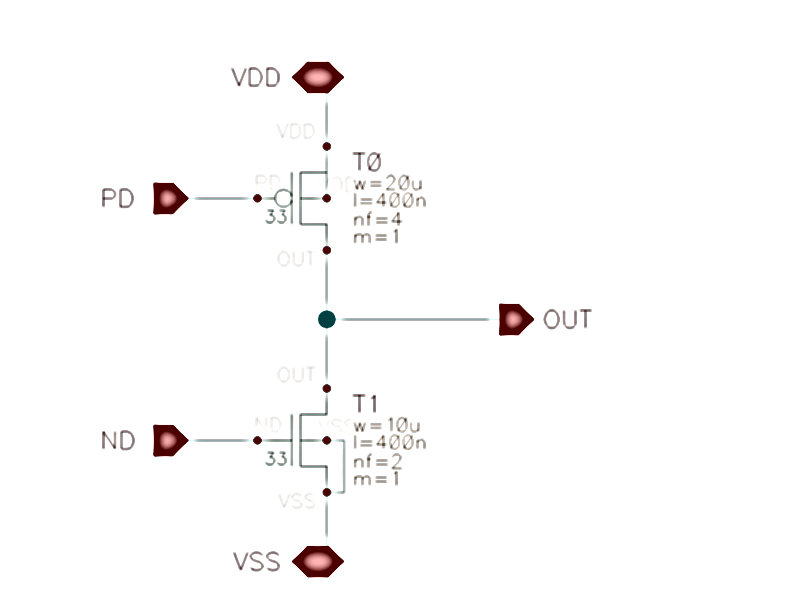


Figure 5: Split Driver Design

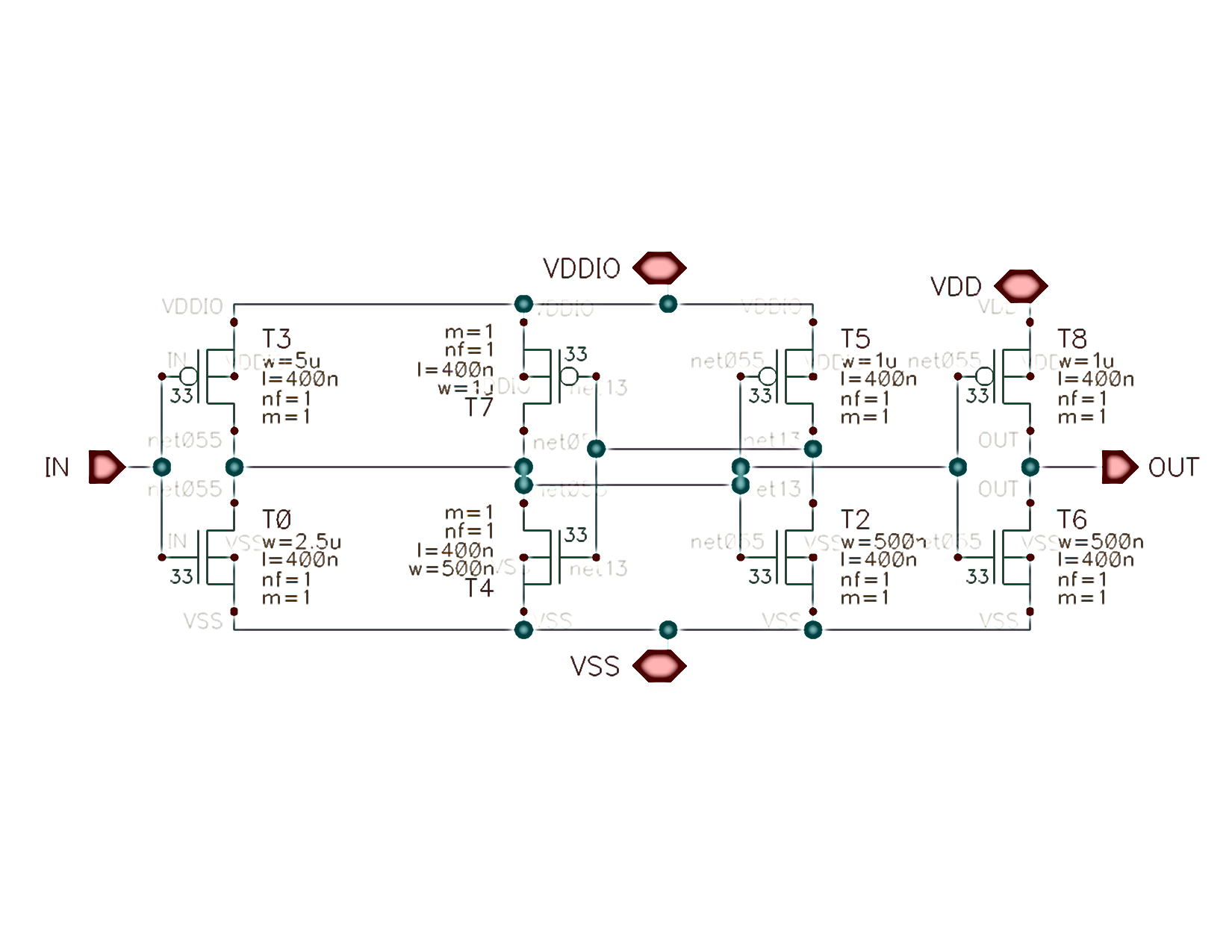
In sizing the final output driver stage we encounter the issue of whether to size our driver to match the transmission line impedance or to simply delivery the necessary output at a given frequency. As a result of the calculations performed in the chip-to-chip channel model portion of this write up we will consider the later.

A number of simulations were carried out before the project proposal to determine that an NMOS width of 10µm (PMOS of 20µm) provided the necessary drive strength. This is approximately half the size required to produce an on resistance of 130Ω at the output of the device (HF match). These are included in the following section.

## Input Buffer Design

### Simple Input Buffer Design

We began with a simple input buffer that allowed us to better understand how this type of circuit works. This design contains an inverter that functions at the communication voltage that connects to a CMOS Schmitt Trigger, connecting to a final inverter that operates at the internal logic voltage of the chip.

  
Figure : Simple Input Buffer Design

As shown above, the simple buffer design contains three stages of logic, each only containing two transistors in series. This proves to become a problem when looking at leakage, as more transistors in series prove to reduce leakage. This lead us to continue studying input buffer designs and look for one that is more suitable for us.

### Final Input Buffer Design

The 12T input buffer design was created around the idea of the Schmidt trigger used in the simple input buffer, with a few improvements. This design contains hysteresis, making the circuit act like it has a strong PMOS while being pulled down and a strong NMOS when being pulled up. This is independent of the rate of change of the input, allowing us to create a VTC plot showing the difference in an upwards transition and a downwards transition. This design filters out noise that might occur due to interference outside of the chip.

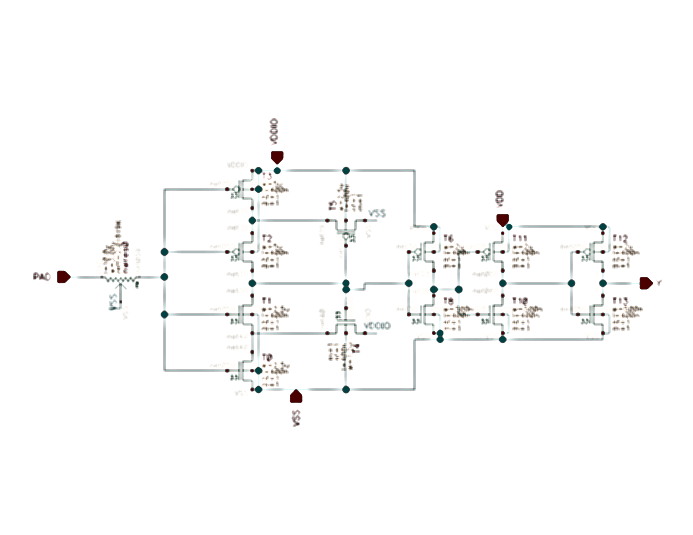


Figure : Final Input Buffer Design

With this design, the NMOS and PMOS transitions are not equal in switching time, as shown in Figure 26. This is due to the VDDIO inverter on the output having a much higher VM than the inverters on VDD. This cannot be fixed by resizing the transistors in the circuit because the NMOS transistor does not turn on until the input on the VDD inverter reaches approximately 250mV, so the output of this design will always be limited by tphl. This switching time is not affected by the input voltage, as shown in Figure 27.

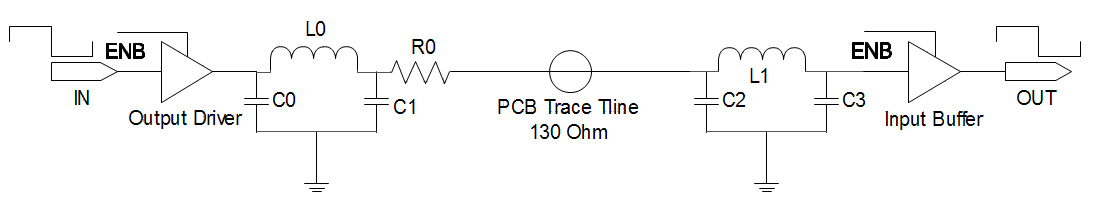
When analyzing the circuit, it is good to look at one group of transistors at a time, either the PMOS in the first stage, or the NMOS in the first stage. If you examine the pull up network during a falling input, you can see that the PMOS transistors on the left turn on after the input approaches VDDIO – Vt. The gate of the third PMOS functions as a negative feedback loop, fighting the pull up of the output, until the gate eventually turns it off, allowing the full swing to complete. These additional transistors create the filtering function of the Schmidt trigger. This output is then level converted to VDD using transistors that can handle the higher voltage at their gates while operating at the logic voltage level.

The power attributes of this circuit make it excellent for low power applications. First and foremost, the added hysteresis feature does not create any static current in the circuit. As long as the input contains a full swing between VDDIO and VSS, the gates on one side of the pull up or pull down network will be turned off. Another nice attribute of this design is that some of the transistors are stacked in series, reducing leakage. Lastly, we chose this circuit because it has a very wide range of acceptable input voltages, allowing for the circuit user to decide between compliance and low power operation while not being required to use a new circuit.

# Revised Plans and Progress

As a result of time constraints and further discoveries that occurred during the design space exploration and power reduction stages the original design plan (as described in the project proposal has been slightly modified).

Rather than focusing on system integration and synthesizing SPI logic for system control, we will instead use a common SPI-core and focus on driver design and the channel model. Since preliminary results indicate SPI power will be dominated by the buffer (both in active and leakage modes) we can make the argument that this is the place where we might offer the greatest improvement in SPI power consumption and energy per bit.



**Original Control-Based Test Plan**

**Current Physical Test Plan**

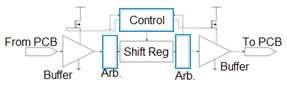


Figure 8: Modified Schematic for Top-Level Testing

As a result the designs stages as described in the project proposal have been modified to include only 4 stages whose descriptions are as follows:

1. Design space exploration
2. Power management and reduction
3. Simulation and analysis with SPI core
4. Iteration and refinement

The preliminary (from the project proposal) and current, revised stage schedule are included below. This is intended to both summarize the reorganization summarized above and also to provide a progress update to this point in the project.

# References

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11. Al-Sarawi, S.F., "Low power Schmitt trigger circuit," Electronics Letters , vol.38, no.18, pp.1009,1010, 29 Aug 2002.
12. *CMOS Schmitt Trigger—A Uniquely Versatile Design Component*. N.p.: Fairchild Semiconductor, June 1975. PDF. http://www.fairchildsemi.com/an/AN/AN-140.pdf

# Appendix A: Simulation Results

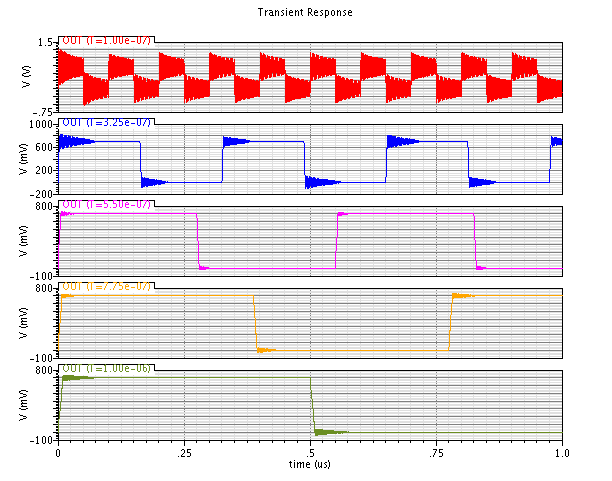
This section includes new simulation results detailing the operation of the designs described above.

## Chip-to-Chip Communication Channel

The chip-to-chip channel model was simulated to some extent prior to design 1 for determination of operating region. By sweeping trace length and operating frequency we can characterize the effects of physical and electrical length of the PCB trace on the operation of the channel.

### Transient Response over Various Operating Frequency (trace length = 5cm)

The simulation below shows the qualitative decay of the signal quality as the frequency of operation increases. It is worth noting that in this weak-driven simulation the output of the driver stage crosses VM for a simple input buffer multiple times during a single transition at 10 MHz, resulting in input glitching if not carefully managed.



10 MHz

3.07 MHz

1.8 MHz

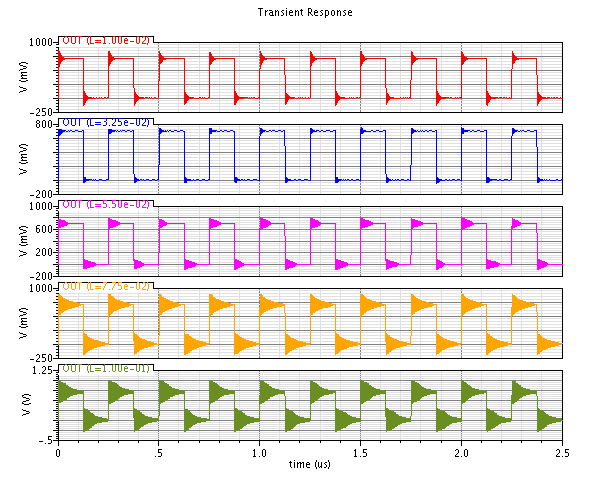
1.3 MHz

1 MHz

Figure 9: Output Signal versus Operating Frequency

### Transient Response over Various Physical Length (f = 4MHz)

The simulation below shows how the quality of the output signal decays as the electrical length of the transmission line grows (reflection magnitude and line delay both increase linearly).



3.25 cm

1 cm

5.5 cm

7.75 cm

10 cm

Figure 10: Output Signal versus Physical Length

## Output Buffer

Both the simple and more complex (tri-stated) output buffers were designed in IBM 130nm technology and simulated to produce sizing for the final output stage, peak active and leakage currents, propagation time, and response to various load cap. Results are included below.

### Output Buffer Width versus Drive Strength

The output buffer sizing for low-frequency operation was determined according to a frequency sweep and qualitative evaluation of the signal rise and fall time in regard to clock period. The width of the NMOS device was swept from 1µm to 10µm and the following simulation results were obtained at an operating frequency of 5MHz.

3.25 µm

1 µm

5.5 µm

7.75 µm

10 µm

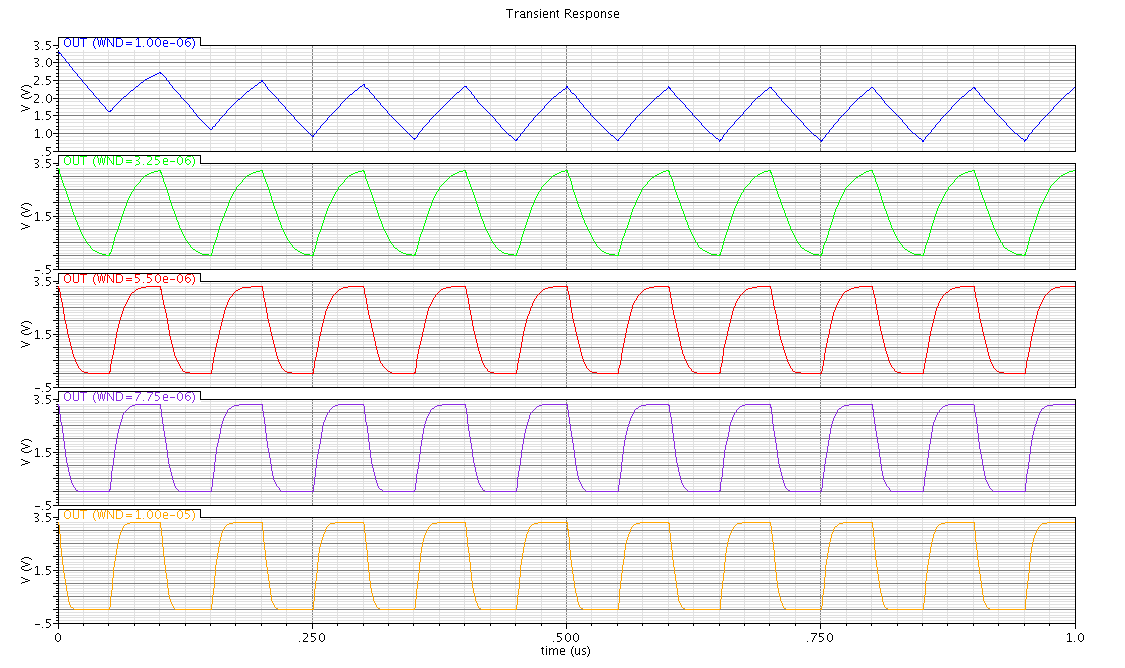


Figure 11: Output Signal versus Driver Size

As a result of this simulation a final NMOS size of 10µm was decided upon. Though 5 MHz is above the targeted frequency of operation this distortion of the input waveform at this operating frequency gives us a nice guard-band for real-world operation in the presence of noise and variation.

### Simple Output Driver Active and Leakage Current

The simulated peak active and leakage currents for 500mV input and 3.3V output (worst-case) are plotted below. It is worth noting that this simple driver was sized to have an input impedance of 130Ω, not with the minimum NMOS width arrived at in the previous simulation.

Current from VIO

Current from VDD

OUT

IN

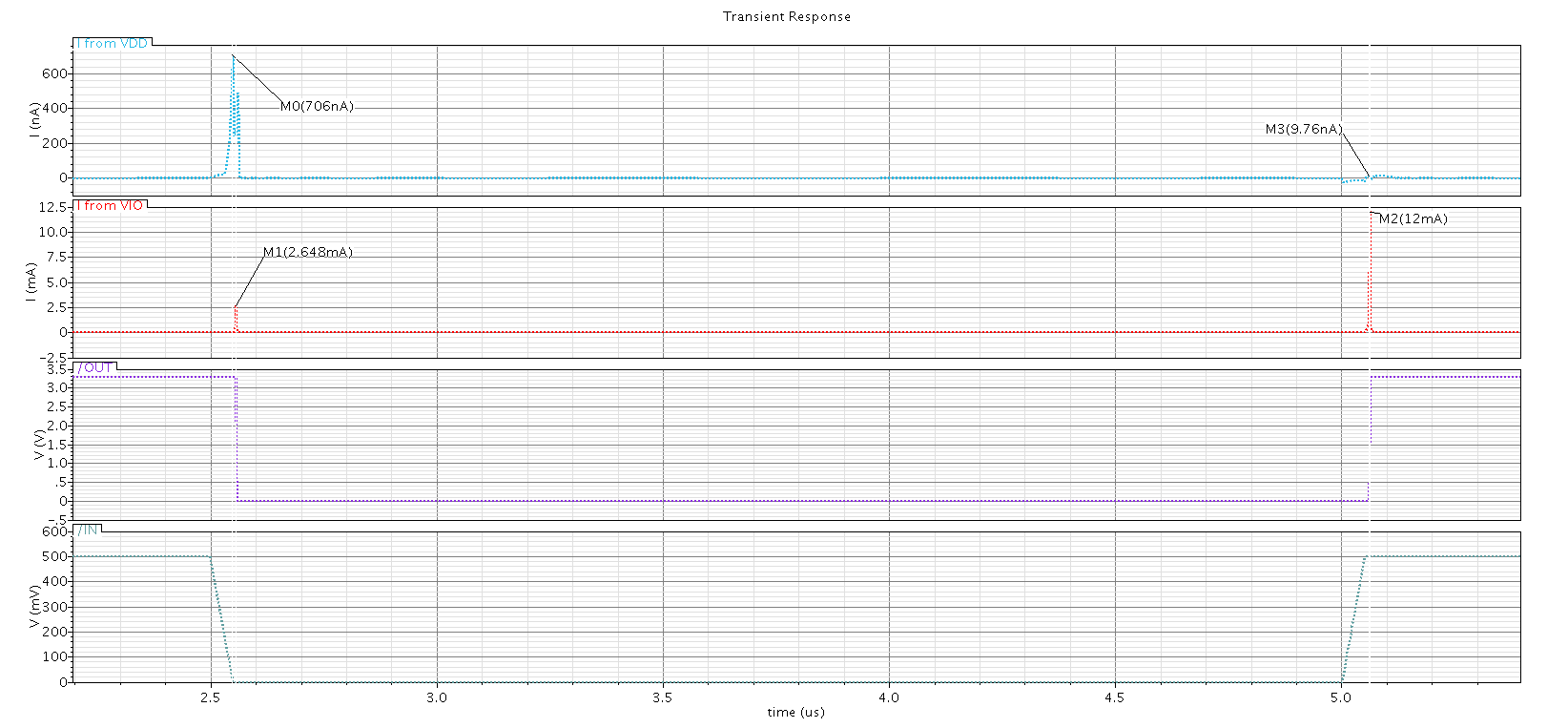


Figure 12: Simple Output Driver Peak Active Current

These peak values will be compared with those of the more advanced final driver design, which is sized based upon the NMOS width derived above. Based on the results below we can see that this design draws about 2.65mA of peak current on a high-to-low transition and 12mA of current on a low-to-high transition.

OUT

Current from VIO

Current from VDD

IN

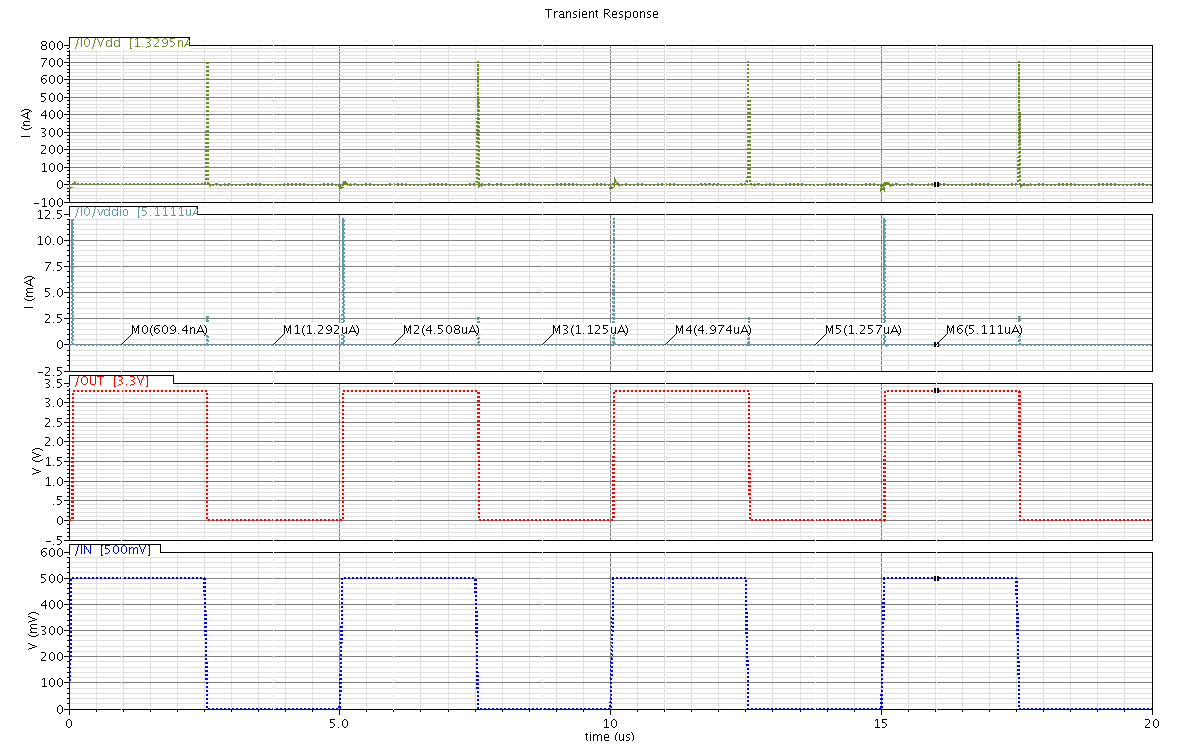


Figure 13: Simple Output Driver Peak Leakage Current

### Simple Output Driver Propagation Time over VIO

Next, the tphl and tplh for the simple output driver was characterized for various voltage outputs ranging from 500mV to 3.3V at the output. In each case the effect of changing VIO on the propagation time was recorded. These results are included below.

1.2V

1.9V

2.6V

3.3V

IN

500mV

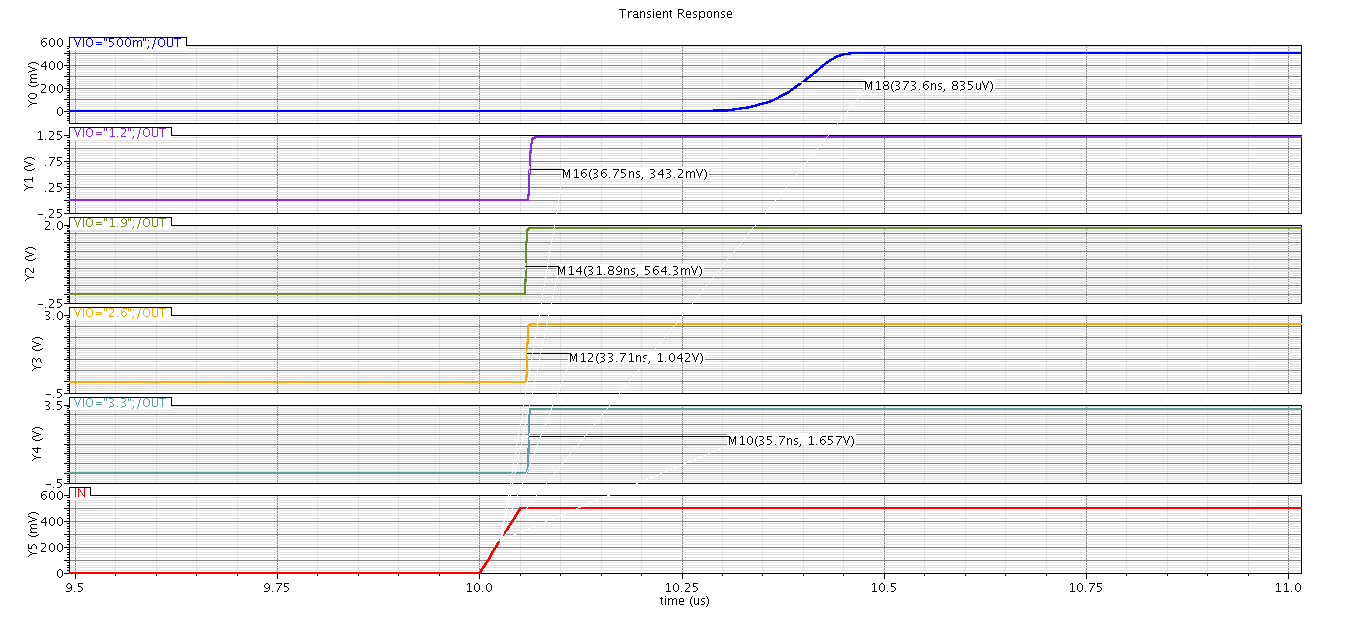


Figure 14: Simple Output Driver Tplh for Various VIO

500mV

1.2V

1.9V

2.6V

3.3V

IN

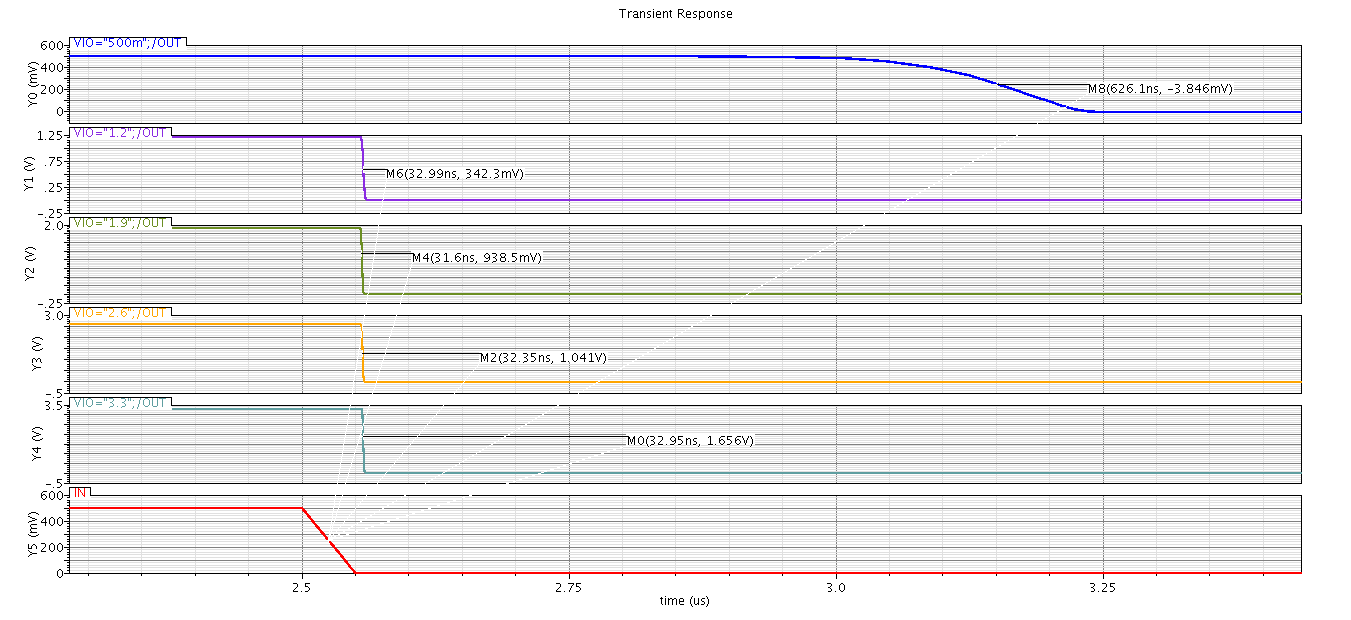


Figure 15: Simple Output Driver Tphl for Various VIO

Here we can see that the low-to-high and high-to-low propagation time is significantly affected by the output voltage of the circuit. For VIO = 1.2, 1.9, 2.6, and 3.3V the propagation time decreases with voltage (as here the 3.3V FETs are operating the super-threshold region and have to charge the output cap less). However, when VIO = 500mV the output takes a great deal longer to propagate as the output buffer is working in the deep sub-threshold regime.

### Simple Output Driver Propagation Time over VDD

In addition to observing the effect of VIO (the driver output voltage) on tphl and tplh, the simple output driver was also characterized for various internal logic voltages (VDD) ranging from 500mV to 1.2V at its input. In each case the effect of changing VDD on the propagation time was recorded. These results are included below.

500mV

675mV

850mV

1.02V

1.2V

IN

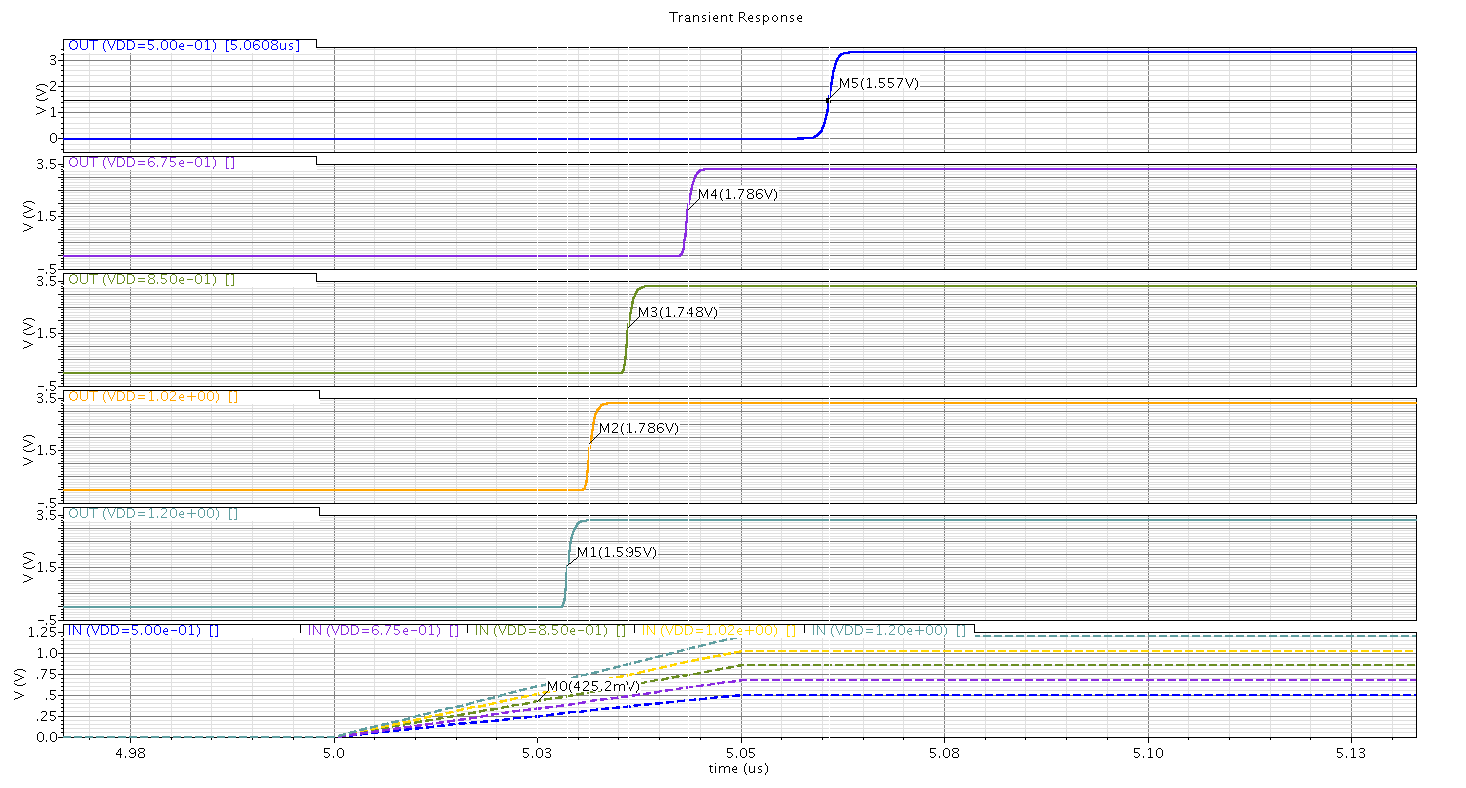


Figure 16: Simple Output Driver Tplh for Various VDD

500mV

675mV

850mV

1.02V

1.2V

IN

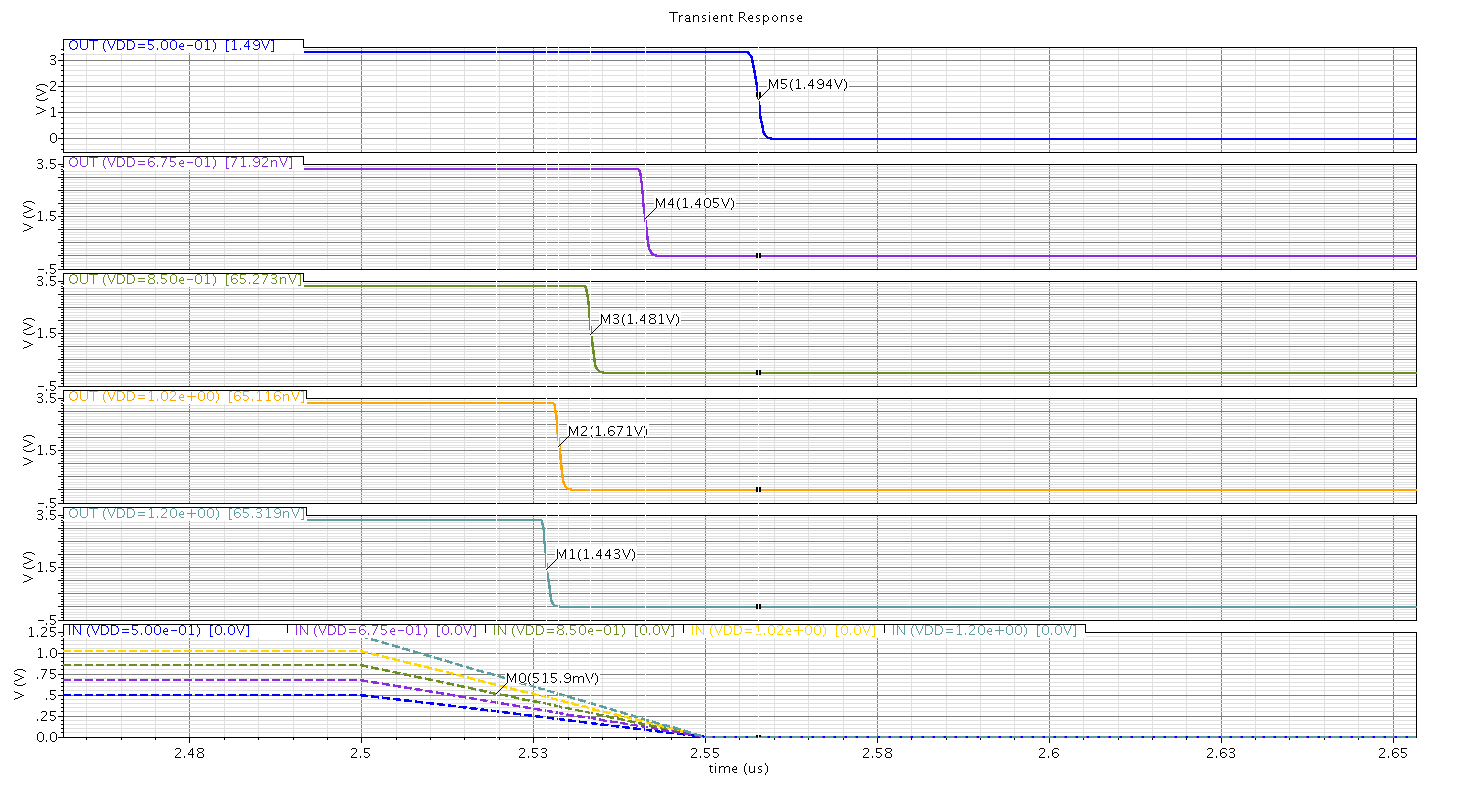


Figure 17: Simple Output Driver Tphl for Various VDD

Here we see that by increasing the internal supply voltage (bringing the LVT control logic further into super threshold operation) we get faster convergence of the output. Thus, as expected, we can increase the internal supply voltage (VDD) in order to run the output driver at higher frequencies.

### Final Output Driver Behavioral Simulation

First and foremost the final output driver’s logical function was tested using a simple combination of the input and tri-state control pins. A SPICE simulation capturing the correct behavioral operation of the element is included below.

IN

3S

OUT

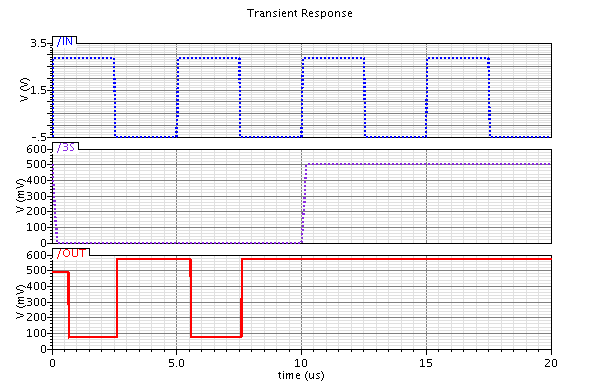


Figure 18: Final Output Driver Behavioral Simulation Results

As we can see the output tracks the input when the tri-state input is low. When the tri-state goes high the output is electrical un-driven and floats up near the previous value of the bus (‘1’ before tri-stating). Towards the tail end of the figure (20µs mark) we can start to see the effect of leakage as the output voltage begins to sag slightly.

### Final Output Driver Active and Leakage Current

The results of the sizing simulation summarized above were now used to size the output buffer rather than HF input impedance (as used in the simplistic driver design). Once this final split-drive stage had been sized, the peak active and leakage currents for this new design, in the active and tri-state modes, were simulated. The results of this simulation are included below.

Current from VDD

Current from VIO

OUT

IN

3S

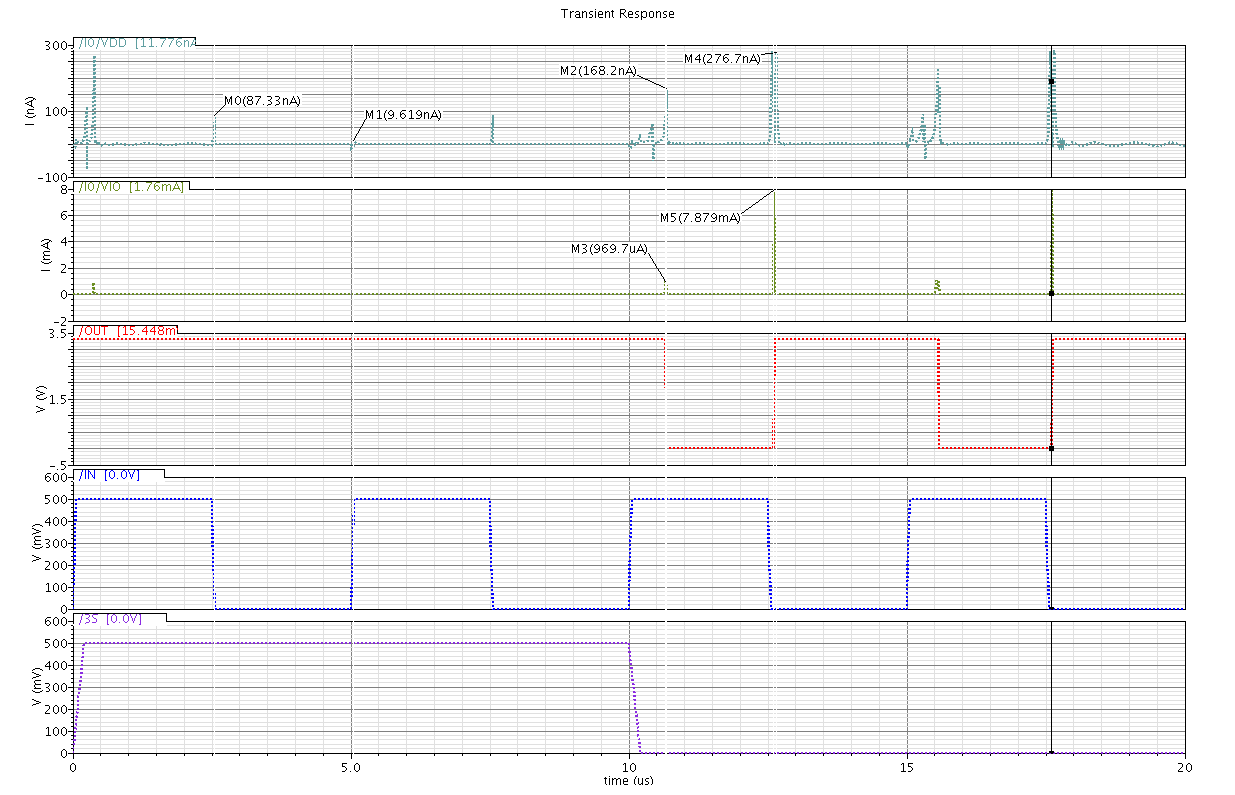


Figure : Final Output Driver Peak Active Current

Current from VDD

Current from VIO

OUT

IN

3S

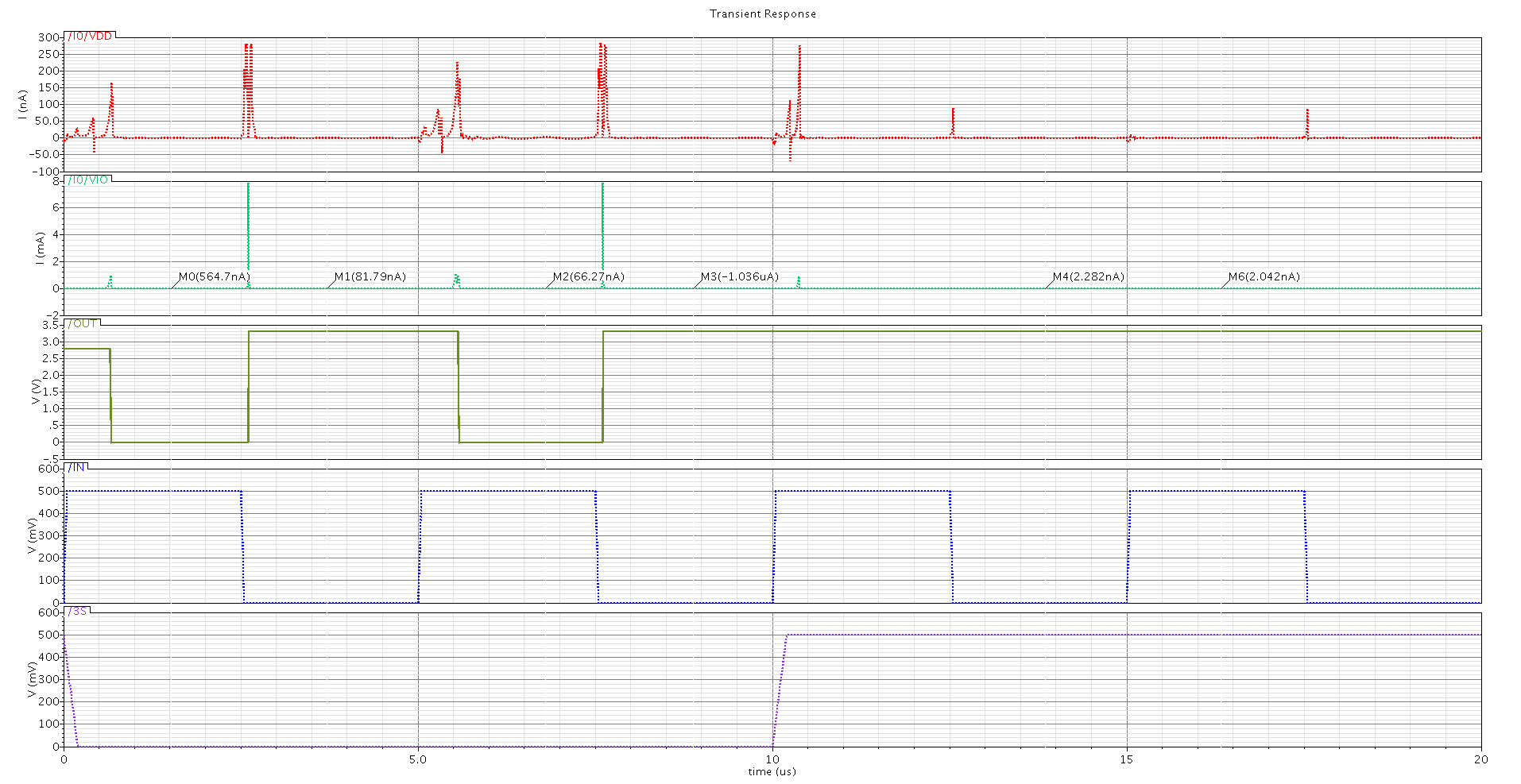


Figure 20: Final Output Driver Peak Leakage Current

As we can see in the results above, using the split-driver topology reduced peak active current only slightly (down to about 1mA high-to-low and 8mA low-to-high), but took worst-case leakage current from 2µA down to about 2nA during tri-state shutdown. This 6 order-of-magnitude decrease in leakage current is considered a significant improvement on the previous buffer design and one of the biggest successes of the power reduction stage of design.

### Final Output Driver Propagation Time over VIO

Similarly to the simple driver, the tphl and tplh for the final output driver was characterized for various voltage outputs ranging from 500mV to 3.3V at the output. In each case the effect of changing VIO on the propagation time was recorded. These results are included below.

IN

500mV

1.2V

1.9V

2.6V

3.3V

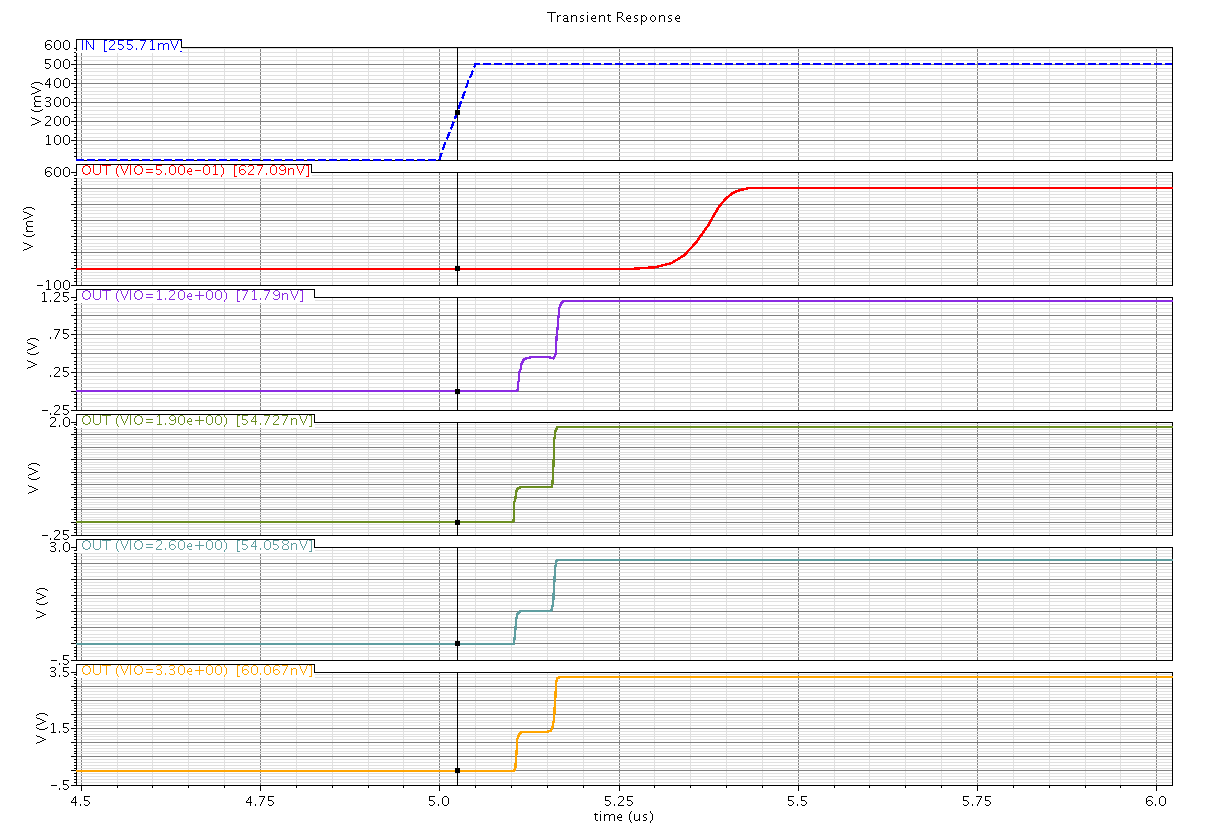


Figure 21: Final Output Driver Tplh for Various VIO

IN

500mV

1.2V

1.9V

2.6V

3.3V

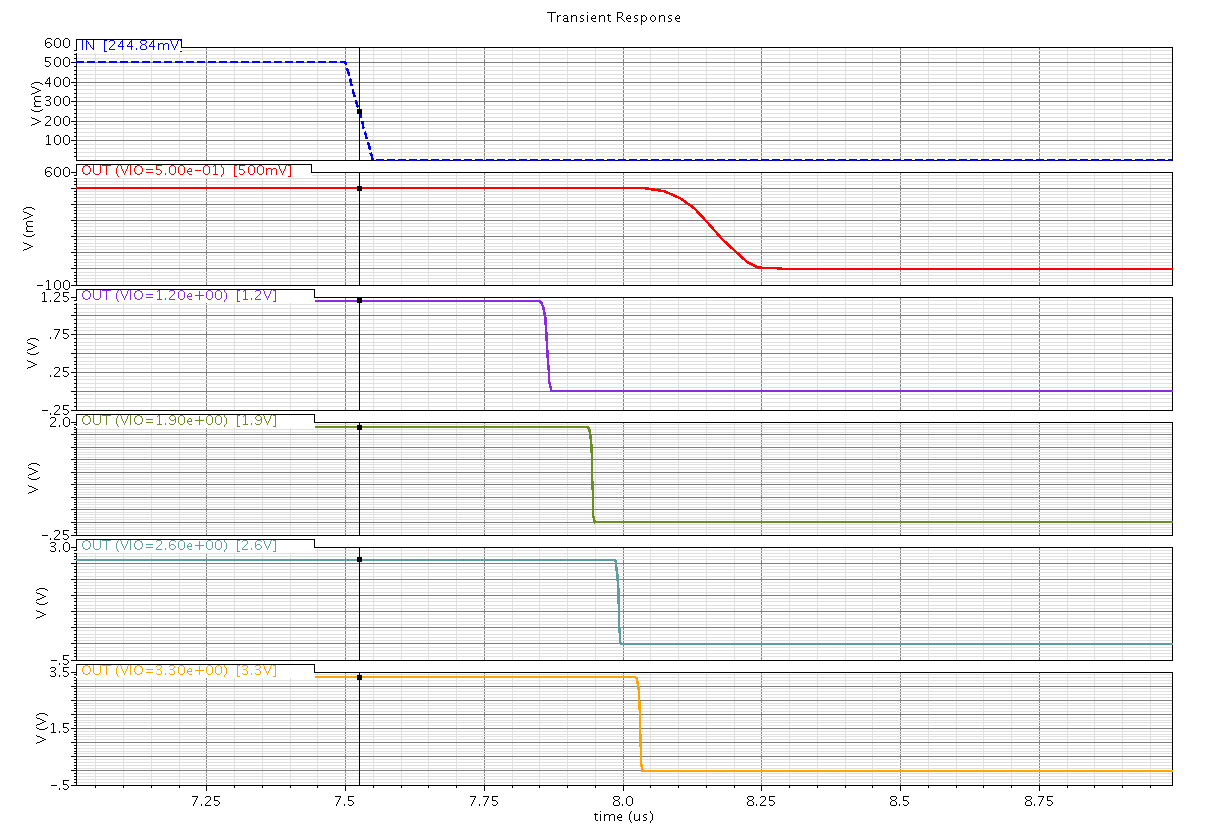


Figure 22: Final Output Driver Tphl for Various VIO

Again, similarly to the simplistic output driver, we see the effect of lowering the output voltage (VIO) as decreasing tphl and tplh until the 3.3V FETs enter the sub-threshold region and produce the largest delay at the lowest voltage 500mV.

### Final Output Driver Propagation Time over VDD

Also analogously to the simple driver design, the effect of VDD (the internal logic voltage) on tphl and tplh was also characterized for the final driver design. In each case the effect of changing VDD on the propagation time was recorded. These results are included below.

IN

500mV

675mV

850mV

1.02V

1.2V

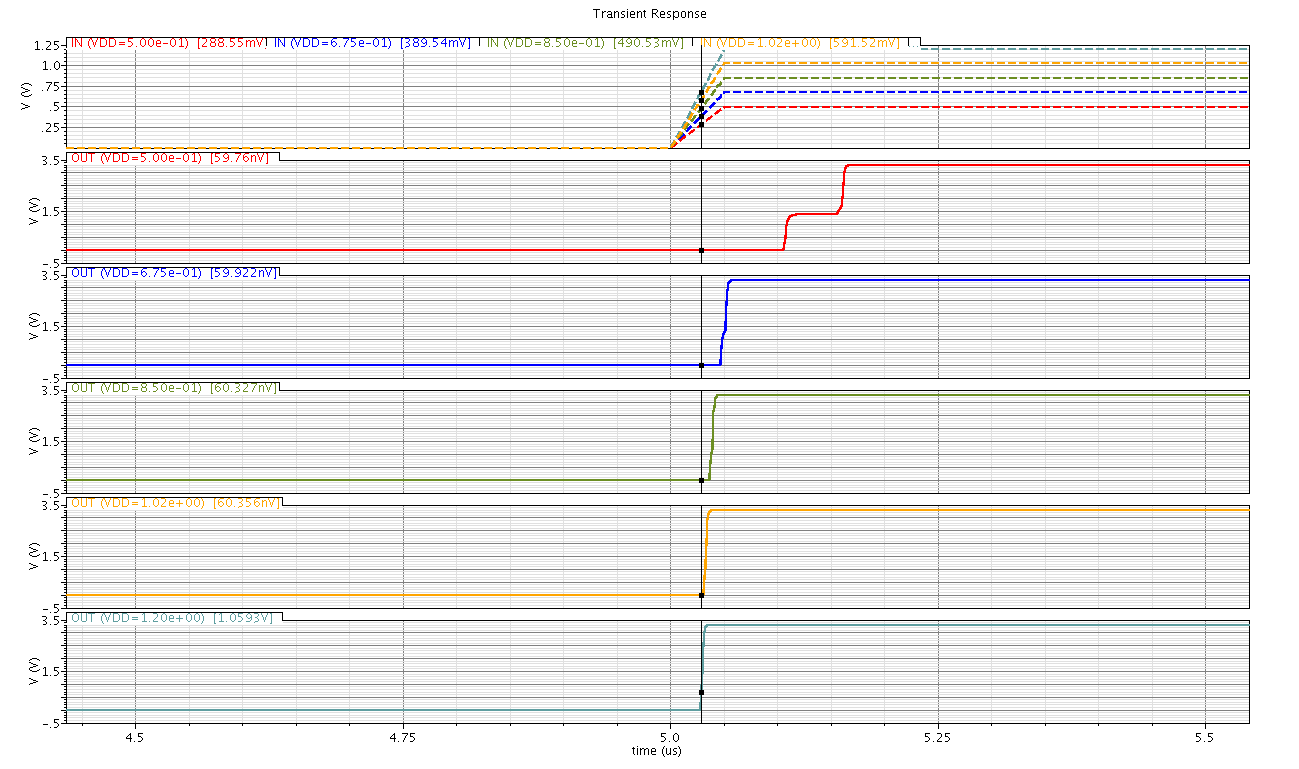


Figure 23: Final Output Driver Tplh for Various VDD

IN

500mV

675mV

850mV

1.02V

1.2V

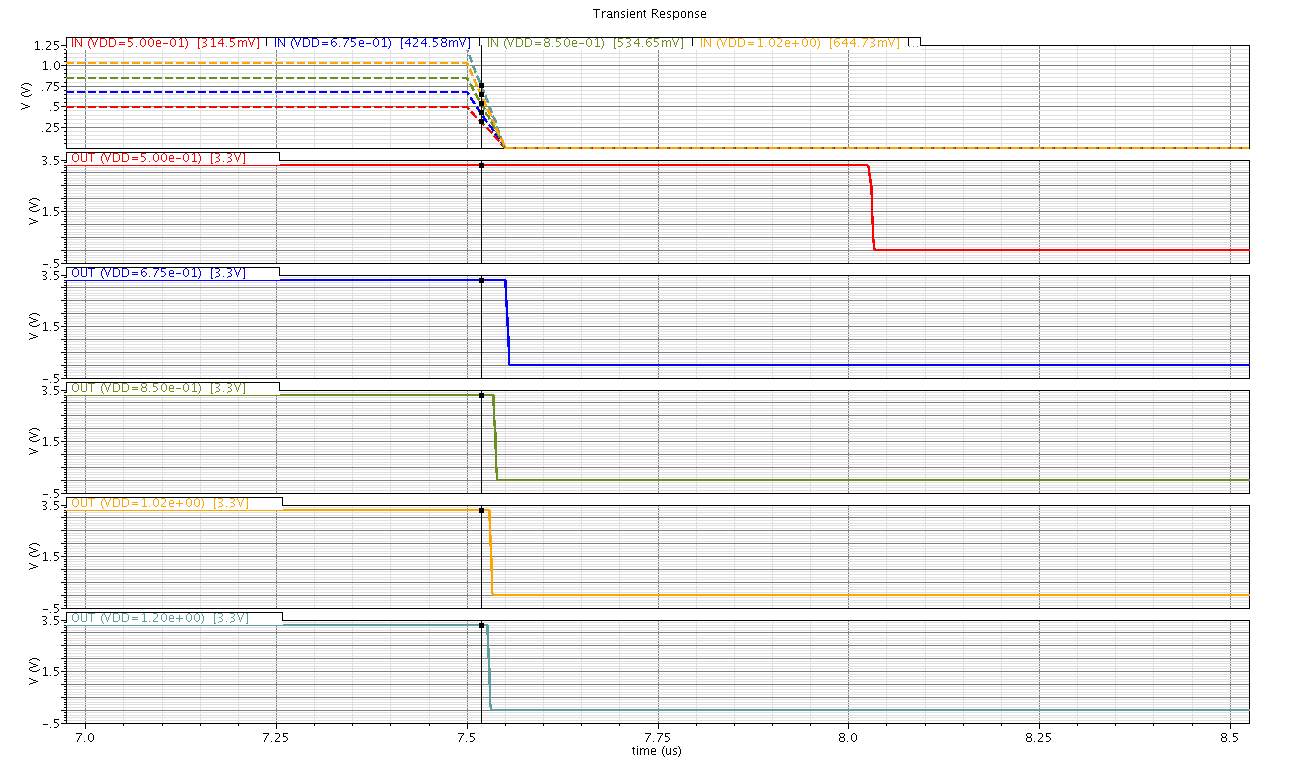
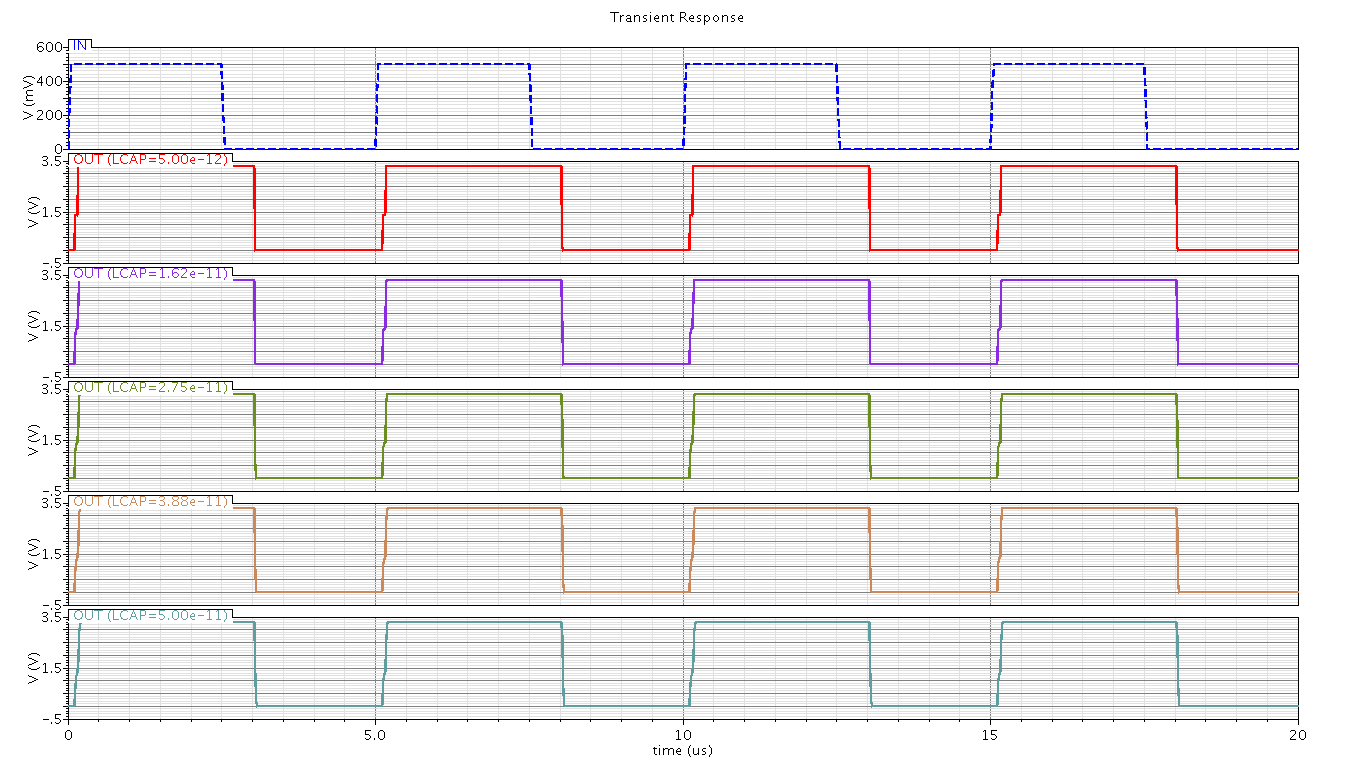


Figure 24: Final Output Driver Tphl for Various VDD

We see a very similar trend in the effect of propagation time of tplh and tphl in this circuit. One noticeable difference in these simulations is the stair-step effect seen in the 500mV tplh signal. This is an effect of propagation time in standard cell logic affecting the split-drivers output convergence and can be minimized with careful timing of these signals. Alternatively, this effect can be used to our advantage to greatly reduce the effect of any potential short-circuit currents on circuit operation.

### Final Output Driver over Various Load Cap

As a last sanity check of the final output driver design the input and output voltages were held constant (500mV and 3.3V respectively) and a sweep of the output load cap (5-50pF) was performed. Results are included below.

50pF

38.8pF

27.5pF

IN

5pF

16.2pF

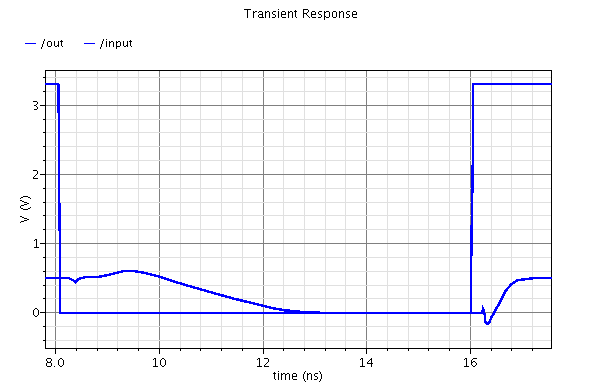
Figure 25: Final Output Driver for Various Load Cap

As we can see in the figure above, the effect of load cap on circuit operation is somewhat minimal at an operating frequency of 200 kHz (the minimum targeted throughput). This is preferable as it means small changes in the characteristics of the pad, bond wire, or trace model will not necessarily cause the driven output to fail.

## Input Buffer

### Converting from 3.3 V to 500 mV

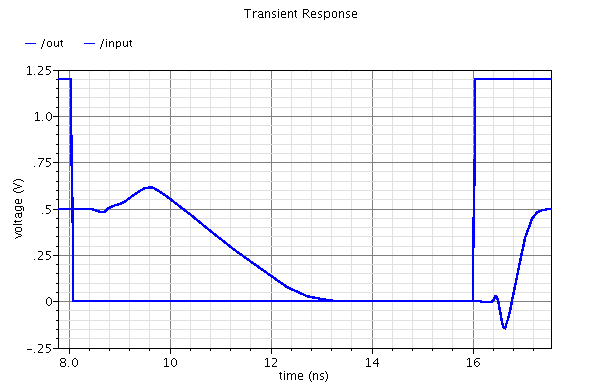
The input buffer both filters the incoming signal and converts the voltage from the outside world into 500 mV. This allows for subthreshold operation inside the chip while still communicating at a standard voltage. The figure below shows the transition times for an input voltage of 3.3V.

  
Figure : Transition Times for a 3.3 Volt Input and a .5 Volt Output

It is notable that the transition time from high to low is higher than the transition time from low to high. This is the case because Vm of the output inverters is much lower than Vm of the high voltage inverter. This results in a delay in the last inverter switching because the switching process doesn’t begin until the high voltage inverter is almost completed switching. The transition time from low to high is much lower because the output inverter begins switching at the beginning of the low to high transition of the high voltage inverter. I found Tplh to be approximately 600 ps, while Tphl was 3.12 ns for a 3.3V input.

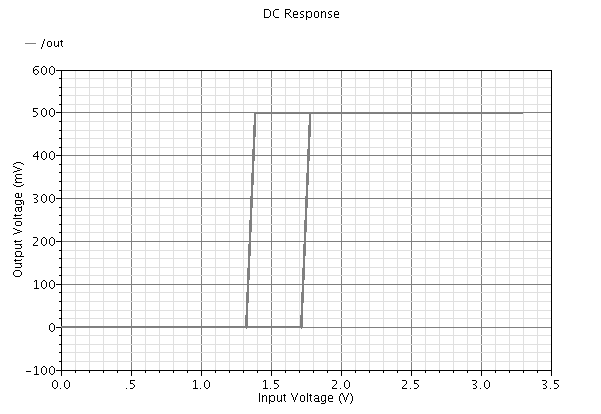
### Converting from 1.2V to 500mV

The transition time changes very little when changing the voltage of operation at the input, as seen in the figure below. The ratio of Tplh and Tphl stays the same, while occurring at a little slower rate. This is because the functionality of the circuit does not change. Tplh was found to be 910 ps, while Tphl was 3.35 ns for the 1.2V input operation.

  
Figure : Transition Times for a 1.2 Volt Input and a .5 Volt Output

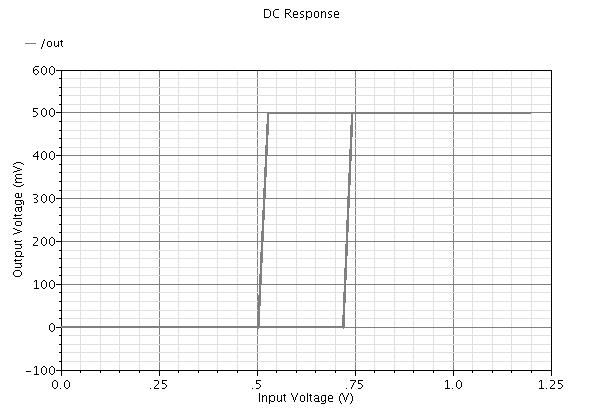
### Hysteresis of 3.3V operation

The 3.3 volt operation shows around a .4V separation between the high to low transition and low to high transition. It is well balanced around what would be considered an ideal Vm of 1.5V. In the below image you can see both transitions. The lower voltage transition is the high to low transition, while the higher voltage transition is the low to high transition. The transition from high to low occurs at a 1.35V input, while the transition from low to high occurs at 1.75V.

  
Figure : Hysteresis Simulation at an Input of 3.3V

### Hysteresis of 1.2V operation

The 1.2 volt operation works very similarly to operation at 3.3 volts. The main change that occurs is the width of the Hysteresis. The width changes from 400mV to just above 200mV. I found the transition from high to low to occur at a 516mV input, while the transition from low to high occurs at 732mV.

  
Figure : Hysteresis Simulation at an Input of 1.2V